INDIAN INSTITUTE OF ENGINEERING SCIENCE AND TECHNOLOGY, SHIBPUR

B.Tech. 5th SEMESTER EXAMINATIONS, 2021

MICROPROCESSOR BASED DESIGN (CS 3103)

[Answer script header should have the i) Name, Examination Roll No, G-suit-id]

**Answer question no. 1 and any four from the rest**

Time: 90 Minutes Full Marks: 70\*

[\* To be scaled down to 50 by multiplying with a factor of 5/7]

1. (Answer all) [ 4 x 5]
2. What happens to the flags (sign, zero AND carry) if you execute the following instruction?

XRA A?

1. Which instruction (single) is safe to use to generate a very small delay?
2. What is bus contention? Explain bus contention with a suitable diagram.
3. What happens if you reset 8085 with the READY line connected to ground?
4. What happens if you reset 8085 CPU chip without any other connection (except the power supply—ground)?
5. (a) What is *wait state*? Draw IOW cycle with one wait state. [8]

(b) Write a subroutine in assembly language that converts an 8-bit Gray number to corresponding Binary. The subroutine gets the 8-bit Gray in Acc register and returns the equivalent Binary also through Acc register. Show the calling of this conversion function from the main routine as well. [7]

1. Write subroutines, namely, [7.5 + 7.5]
2. PACK which packs two BCD digits available in B and C registers. Result should be returned through Acc register; and
3. UNPACK which unpacks two packed BCD digits available in Acc to B and C registers. Note the higher and lower nibbles should be returned through B and C registers, respectively.
4. (a) Consider the following segment (X86)

Mydata segment

Name db “CST”

dw 20 dup (?)

Surname db “Department”

Mydata end

What would be the offset of the character ‘m’ appeared in the string Surname from the beginning of the Mydata segment? [5]

1. Draw the decoding hardware necessary to make a D f/f with Enable line acting as an output port (Address 0FAH). No foldback is allowed. Also, add necessary decoding circuitry to avoid undesired output when instruction like

STA 0FAFAH is being executed. [10]

1. a) Tabulate RISC and CISC properties for comparison. [5]
2. Draw the instruction formats of the Berkeley RISC I CPU and show the register window mechanism to reduce the parameter passing overheads [10]
3. a) Draw the programming model of the MCS-48 series microcontroller. For the [7] following program snippet where will the execution control be transferred after the instruction JB3.

L1: MOV A, #157

SWP A

JB3 L1

L2: NOP

b) Discuss the mechanism of picking up the address of an ISR using the vector table in X86 for the software interrupt instruction, say, INT 23H. [8]

1. Suppose an output port (address 80H) bits is driving the segments of a LED module. The connection is tabulated as below. [15]

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| a | b | c | dp | d | e | f | g |

Assuming positive logic construct a display table using appropriate assembler directive and also write subroutines

1. in 8085 assembly that takes octal digits in accumulator and returns the display code through the accumulator; also write
2. the same routine in MCS-48 assembly language